What is Claimed is:

1. A processor comprising:

a plurality of programmable logic arrays (PLAs);

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue.

2. The processor of claim 1 wherein said plurality of PLAs are coupled to a plurality of streaming buffers and said plurality of PLAs are to provide an instruction pointer for a first micro-operation in each instruction and predict a number of micro-operations between the first micro-operation and a last micro-operation in each instruction.

3. The processor of claim 1 wherein said plurality of PLAs are coupled to an alias logic component.

4. The processor of claim 1 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

5. The processor of claim 3 wherein said instruction pointer queue is at least three micro-instruction pointers wide.

6. The processor of claim 1 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor coupled to said four-to-one multiplexer, said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

7. The processor of claim 6 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation read only memory.

8. The processor of claim 1 wherein said micro-operation cache comprises:

an at least 3-wide micro-operation cache to store commonly used micro-operations.

9. The processor of claim 1 wherein said micro-operation memory comprises:

an at least 3-wide micro-operation read only memory to store all micro-operations that can be decoded from an instruction set.

10. The processor of claim 1 further comprising:

a patch cache coupled to said micro-operation cache.

11. A processor comprising:

a plurality of programmable logic arrays (PLAs) to output a first instruction pointer for a first micro-instruction operation in each instruction;

an instruction pointer queue to receive the first instruction pointers;

an instruction pointer sequencing logic/predictor component to predict a next instruction pointer for each instruction;

a micro-operation cache to store a plurality of frequently used micro-instruction operations;

a micro-operation memory to store a plurality of micro-instruction operations; and

a trace pipe (TPIPE) to build a trace of micro-instruction operations for each instruction.

12. The processor of claim 11 wherein each of said plurality of PLAs to receive input from a build pipe.

13. The processor of claim 11 wherein each of said plurality of PLAs receive input from an alias logic component.

14. The processor of claim 11 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

15. The processor of claim 14 wherein said instruction pointer queue is to concurrently provide up to three micro-instruction pointers.

16. The processor of claim 11 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

17. The processor of claim 16 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation read only memory.

18. The processor of claim 11 wherein said micro-operation cache is to store at least 3 micro-operations per set of commonly used micro-operations.

19. The processor of claim 11 wherein said micro-operation read only memory is store at least 3 micro-operations per set of all micro-operations that can be decoded from an instruction set.

20. The processor of claim 11 further comprising:

a patch cache to store micro-operations and to be read in parallel with said micro-operation read only memory.

21. A method comprising:

determining a first instruction pointer for a first operation in an instruction;

storing the first instruction pointer;

predicting a next instruction pointer for each additional operation in the instruction;

reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers; and

building a trace of micro-operations using the one or more operations for the instruction.

22. The method of claim 21 further comprising:

storing a plurality of commonly used operations for quick access; and

storing a plurality of micro-operations including said plurality of commonly used micro-operations.

23. The method of claim 21 wherein determining a first instruction pointer for a first operation in an instruction comprises:

determining the first instruction pointer for the first operation in the instruction in a programmable logic array.

24. The method of claim 22 wherein predicting a next instruction pointer for each additional operation in the instruction comprises:

predicting the next instruction pointer for each additional operation in the instruction in a predictor separate from the programmable logic array.

25. The method of claim 24 wherein reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers comprises:

reading the one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers from a cache memory or a read only memory, if the one or more operations are not in the cache memory.

26. A machine-readable medium having stored thereon a plurality of executable instructions to perform a method comprising:

determining a first instruction pointer for a first operation in an instruction;

storing the first instruction pointer;

predicting a next instruction pointer for each additional operation in the instruction;

reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers; and

building a trace of micro-operations using the one or more operations for the instruction.

27. The machine-readable medium of claim 26 further comprising:

storing a plurality of commonly used operations for quick access; and

storing a plurality of micro-operations including said plurality of commonly used micro-operations.

28. The machine-readable medium of claim 26 wherein determining a first instruction pointer for a first operation in an instruction comprises:

determining the first instruction pointer for the first operation in the instruction in a programmable logic array.

29. The machine-readable medium of claim 27 wherein predicting a next instruction pointer for each additional operation in the instruction comprises:

predicting the next instruction pointer for each additional operation in the instruction in a predictor separate from the programmable logic array.

30. The machine-readable medium of claim 29 wherein reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers comprises:

reading the one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers from a cache memory or a read only memory, if the one or more operations are not in the cache memory.

31. A computer system comprising:

a memory to provide program instructions; and

a processor coupled to said memory, said processor comprising:

a plurality of programmable logic arrays (PLAs);

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue.

32. The processor of claim 31 wherein said plurality of PLAs are coupled to a plurality of streaming buffers and said plurality of PLAs are to provide an instruction pointer for a first micro-operation in each program instruction and predict a number of micro-operations between the first micro-operation and a last micro-operation in each instruction.

33. The processor of claim 31 wherein said plurality of PLAs are coupled to an alias logic component.

34. The processor of claim 31 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

35. The processor of claim 31 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor coupled to said four-to-one multiplexer, said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

36. The processor of claim 31 further comprising:

a patch cache coupled to said micro-operation cache.

37. A computer system comprising:

a memory to provide program instructions; and

a processor coupled to said memory, said processor comprising:

a plurality of programmable logic arrays (PLAs) to output a first instruction pointer for a first micro-instruction operation in each instruction;

an instruction pointer queue to receive the first instruction pointers;

an instruction pointer sequencing logic/predictor component to predict a next instruction pointer for each instruction;

a micro-operation cache to store a plurality of frequently used micro-instruction operations;

a micro-operation memory to store a plurality of micro-instruction operations; and

a trace pipe (TPIPE) to build a trace of micro-instruction operations for each instruction.

38. The processor of claim 37 wherein each of said plurality of PLAs to receive input from a build pipe that is coupled to said memory.

39. The processor of claim 37 wherein each of said plurality of PLAs receive input from an alias logic component.

40. The processor of claim 37 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

41. The processor of claim 37 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

42. The processor of claim 37 further comprising:

a patch cache to store micro-operations and to be read in parallel with said micro-operation read only memory.